AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for allocation of resources for a field programmable gate array (FPGA) -based system on a chip (SoC), the method comprising:

selecting a first system component for customizing the FPGA-based SoC;

determining types and quantities of FPGA resources required for implementing the first system component and remaining available FPGA resources for the FPGA-based SoC subsequent to said selection of said first system component; [[and]]

displaying a respective quantity for each type of remaining available FPGA resource for the FPGA-based SoC, and a respective quantity of each type of resource used to implement said first system component;

choosing a second system component to utilize said remaining available resources to facilitate allocation of FPGA ~~FPGA-based SoC~~ resources to the FPGA-based SoC; and

displaying a respective quantity of each type of FPGA resource utilized by said second system component.

2. (Original) The method according to claim 1, wherein said determining step further comprises determining total FPGA-based SoC resources.

3. (Original) The method according to claim 2, wherein said step of determining available resources further comprises computing a difference between said total FPGA-based SoC resources and resources utilized by said selected system component, to yield said determined available resources for the FPGA-based SoC.

4. (Currently Amended) The method according to claim 3, further comprising the step of choosing a third system component that utilizes no more than said available resources when said second system component utilizes more resources than [[that]] said determined available resources, said third system component being an alternative to said second system component.

5. (Original) The method according to claim 4, wherein said step of choosing said third system component further comprises computing total resources utilized by said first system component and said third system component.

6. (Original) The method according to claim 5, wherein said step of choosing said third system component further comprises computing a difference between said determined available resources for the FPGA-based SoC and said computed total resources utilized by said first system component and said third system component.

Claim 7. (Cancelled)

8. (Original) The method according to claim 1, wherein said selecting step further comprises selecting a system component from a group consisting of hardware cores, software cores, hardware core parameters and software core parameters, buses, fixed-function FPGA resources, and user-specified design components.

9. (Currently Amended) A method for allocation of resources for a field programmable gate array (FPGA) -based system on a chip (SoC), the method comprising:

selecting system components for customizing the FPGA-based SoC;

computing types and quantities of FPGA resource usage for implementing said selected system components;

for each of a plurality of types of the FPGA resources and for each of the selected system components, displaying a quantity of the FPGA resource usage for implementing the selected system component and displaying for each of the types of FPGA resources a quantity of the resource not required for implementing the selected system components; and

distributing the FPGA-based SoC system resources among said selected system components according to said computed resource usage to customize said FPGA-based SoC.

10. (Original) The method according to claim 9, wherein said step of computing said resource usage further comprises determining resources to be used by at least one selected system component and determining FPGA-based SoC resources available for use by at least an unselected system component.

11. (Original) The method according to claim 10, further comprising:
if said selected system component requires more FPGA-based SoC resources than said available FPGA-based SoC resources, providing an unavailable resource notification.

12. (Original) The method according to claim 11, further comprising the step of determining at least one alternative system component requiring less resources than said available FPGA-based SoC resources.

13. (Original) The method according to claim 12, wherein said determining step further comprises selecting said determined at least one alternative system component to customize the FPGA-based SoC.

14. (Original) The method according to claim 9, wherein said computing step further comprises determining incompatibility between said selected system components.

15. (Original) The method according to claim 14, wherein said determining step further comprises determining at least one alternative compatible system component for replacing an incompatible system component.

16. (Original) The method according to claim 9, wherein said selecting step further comprises selecting a system component from a group consisting of hardware cores, software cores, hardware core parameters and software core parameters, buses, fixed-function FPGA resources, and user-specified design components.

17. (Original) The method according to claim 16, further comprising the step of selecting a default parameter for said selected system component.

18. (Original) The method according to claim 17, wherein said step of selecting said default parameter for said selected system component further comprises the step of propagating said default parameter throughout said customization of the FPGA-based SoC.

19. (Currently Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of:

selecting a first system component for allocating field programmable gate array (FPGA) resources while customizing a FPGA-based SoC;

determining types and quantities of FPGA resources required for implementing the first system component and remaining available FPGA resources for said FPGA-based SoC subsequent to said selection of said first system component;

for each of a plurality of types of the FPGA-based SoC resources, displaying a quantity of the available resources for the FPGA-based SoC and a quantity of the FPGA resources required to implement the first system component; and

choosing a second system component to utilize said remaining available resources to facilitate allocation of FPGA ~~FPGA based SoC~~ resources to the FPGA-based SoC; and

displaying a respective quantity of each type of FPGA resource utilized by said second system component.

20. (Original) The machine readable storage according to claim 19, wherein said determining step further comprises determining total FPGA-based SoC resources.

21. (Original) The machine readable storage according to claim 20, wherein said step of determining available resources further comprises computing a difference between said total FPGA-based SoC resources and resources utilized by said

selected system component, to yield said determined available resources for the FPGA-based SoC.

22. (Currently Amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of:

selecting system components for allocating resources for customizing a field programmable gate array (FPGA)-based system on a chip (SoC);

computing types and quantities of FPGA resource usage for implementing said selected system components;

for each of a plurality of types of the FPGA resources and for each of the selected system components, displaying a quantity of the FPGA resource usage for implementing the selected system component and displaying for each of the types of FPGA resources a quantity of the resource not required for implementing the selected system components; and

distributing the FPGA-based SoC system resources among said selected system components according to said computed resource usage to customize said FPGA-based SoC.

23. (Original) The machine readable storage according to claim 22, wherein said step of computing said resource usage further comprises determining resources to be used by at least one selected system component and determining FPGA-based SoC resources available for use by an unselected system component.

24. (Original) The machine readable storage according to claim 23, further comprising, if said selected system component requires more FPGA-based SoC resources than said available FPGA-based SoC resources, providing an unavailable resource notification.

25. (Original) The machine readable storage according to claim 22, wherein said computing step further comprises determining incompatibility between said selected

system components.

26. (Original) The machine readable storage according to claim 25, wherein said determining step further comprising determining at least one alternative compatible system component for replacing an incompatible system component.

27. (Original) The machine readable storage according to claim 22, wherein said selecting step further comprises selecting a system component from a group consisting of hardware cores, software cores, hardware core parameters and a software core parameters, buses, fixed-function FPGA resources, and user-specified design components.

Claims 28-33 (Cancelled)

34. (New) The method according to claim 1, wherein the types of FPGA resources include look-up table, flip-flop, block memory, I/O buffer, memory, and processor, and displaying the types and quantities of FPGA resources includes displaying quantities for at least three of the types of FPGA resources.

35. (New) The method according to claim 9, wherein the types of FPGA resources include look-up table, flip-flop, block memory, I/O buffer, memory, and processor, and displaying the types and quantities of FPGA resources includes displaying quantities for at least three of the types of FPGA resources.

36. (New) The machine readable storage according to claim 19, wherein the types of FPGA resources include look-up table, flip-flop, block memory, I/O buffer, memory, and processor, and displaying the types and quantities of FPGA resources includes displaying quantities for at least three of the types of FPGA resources.

37. (New) The machine readable storage according to claim 22, wherein the types of FPGA resources include look-up table, flip-flop, block memory, I/O buffer, memory,

and processor, and displaying the types and quantities of FPGA resources includes displaying quantities for at least three of the types of FPGA resources.